

Y



Fig. 1



000000" 215544000

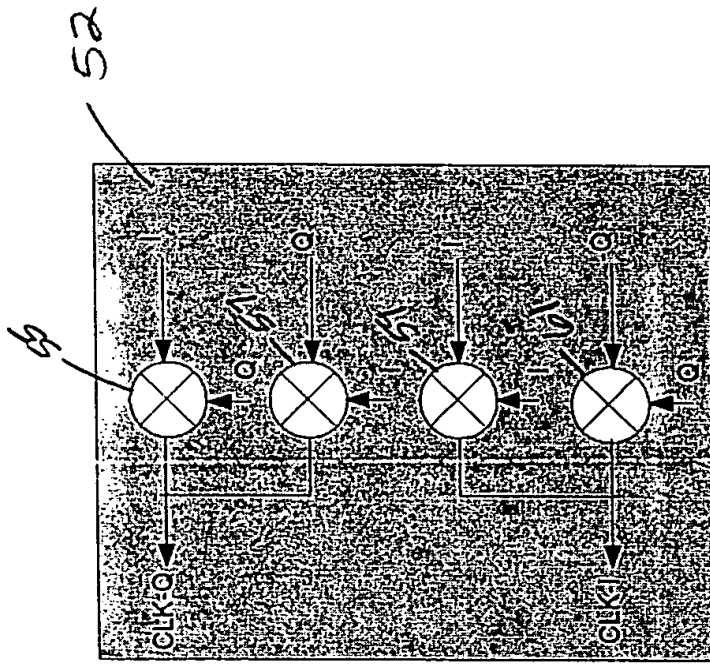


FIG. 3

0363453.030330

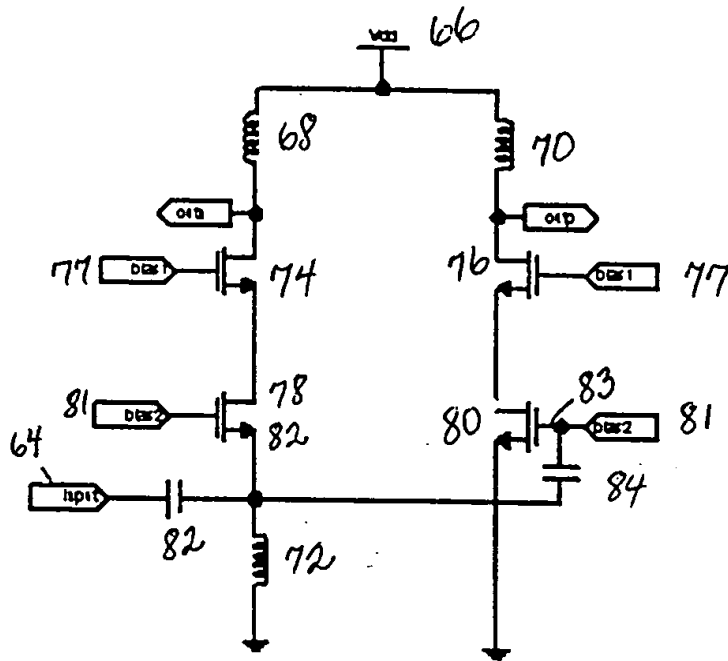


FIG. 4

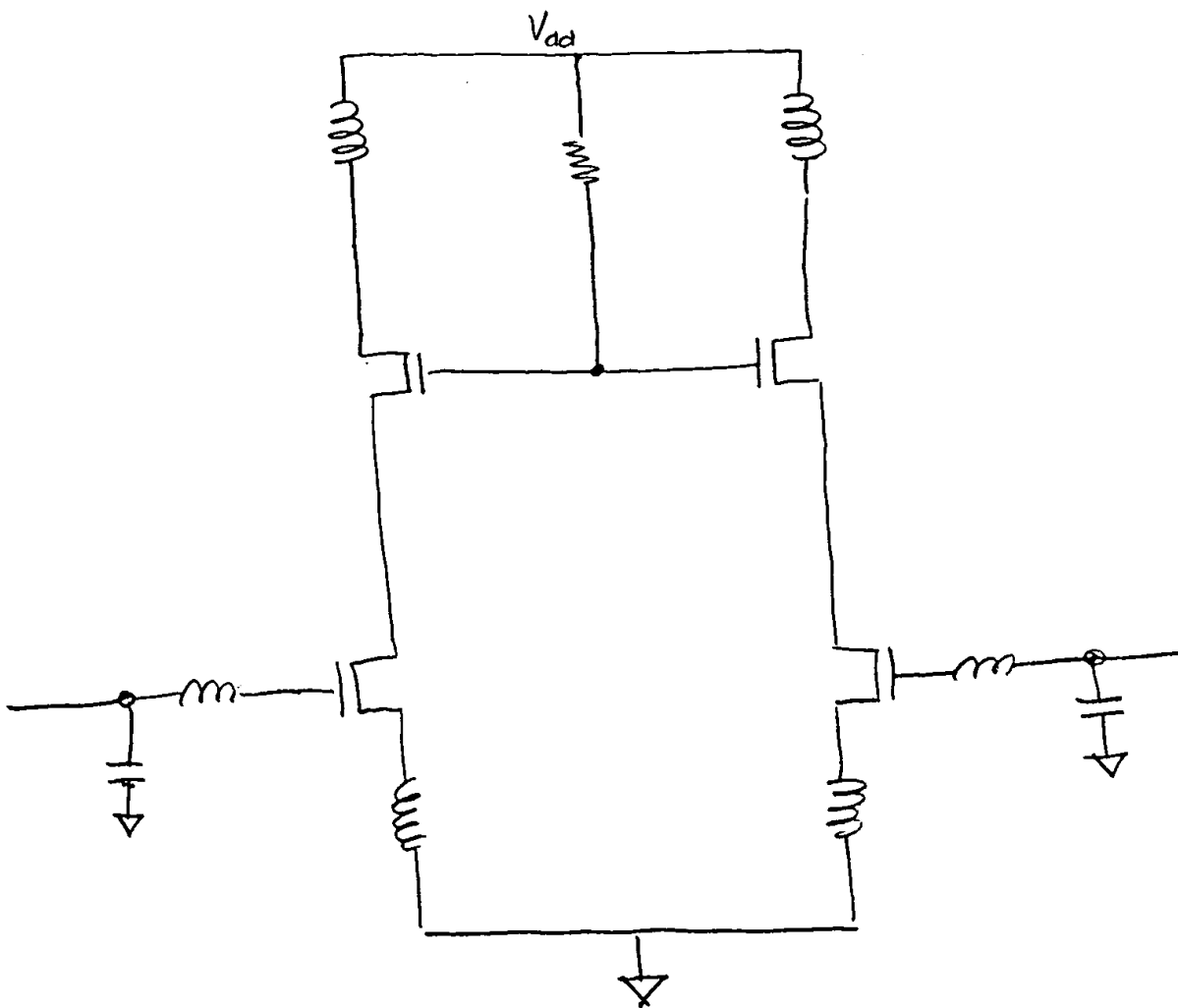


FIG. 4(a)

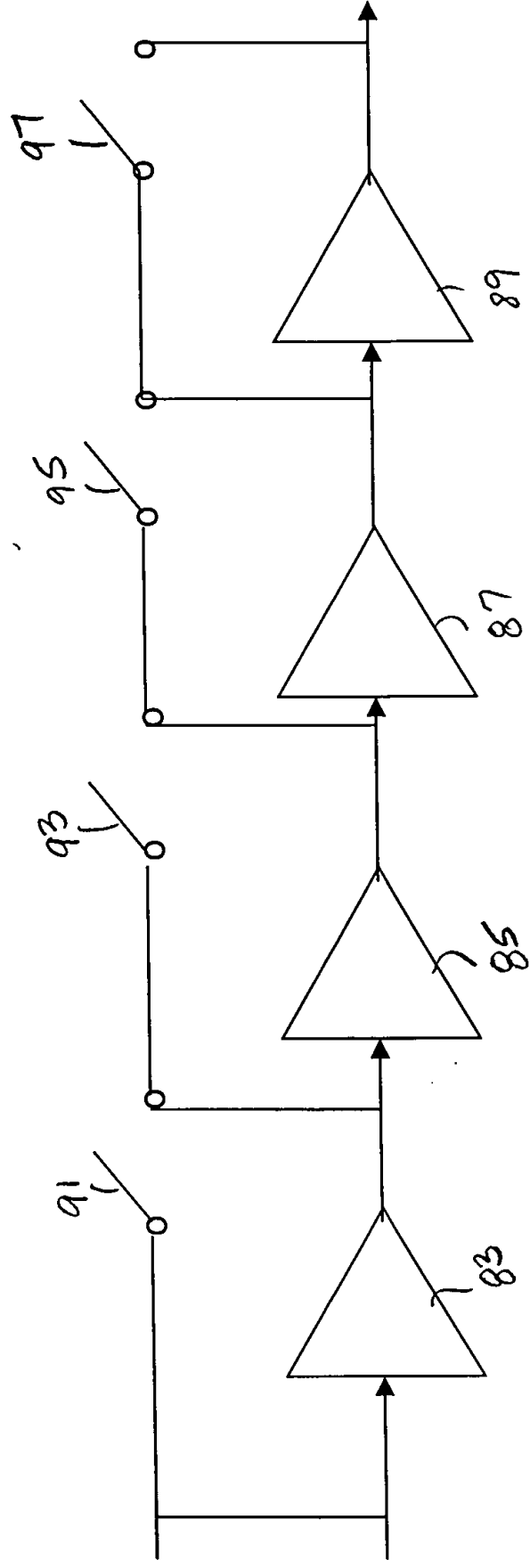


FIG. 5

09534550.000000

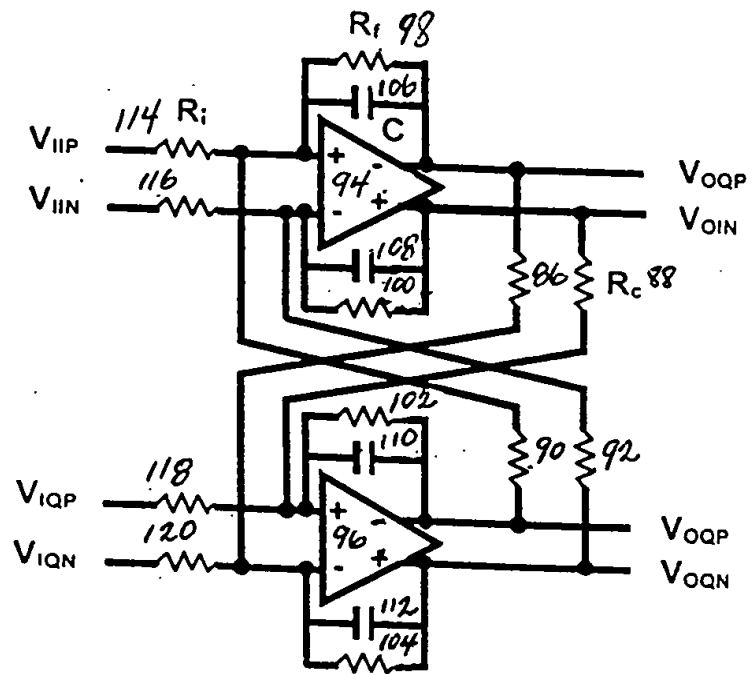


FIG. 6

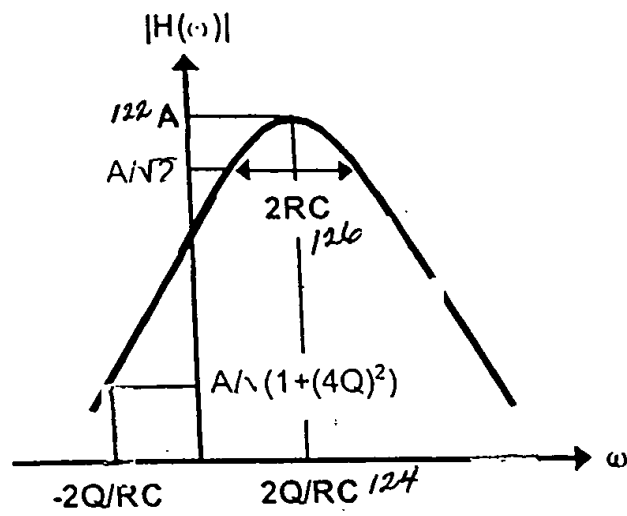


FIG. 7



Diagram for finding  $Y_i$ : A voltage source  $V$  is connected to a parallel combination of a capacitor  $C_z$  (130 pF) and a resistor  $R_z$  (120  $\Omega$ ). The output terminals are shorted to a "Virtual Ground". The current  $I$  is shown flowing into the short. The input admittance is given as  $Y_i = I/V$ .

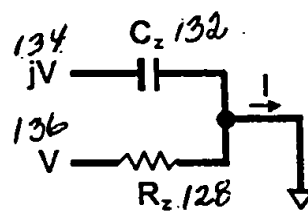


FIG. 9

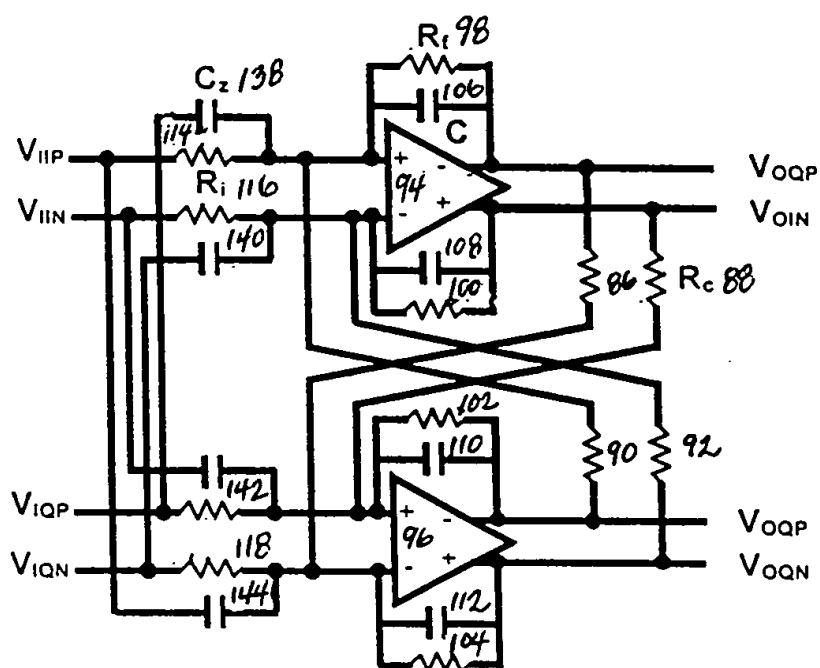
[illegible]

FIG. 10

000000 25442950

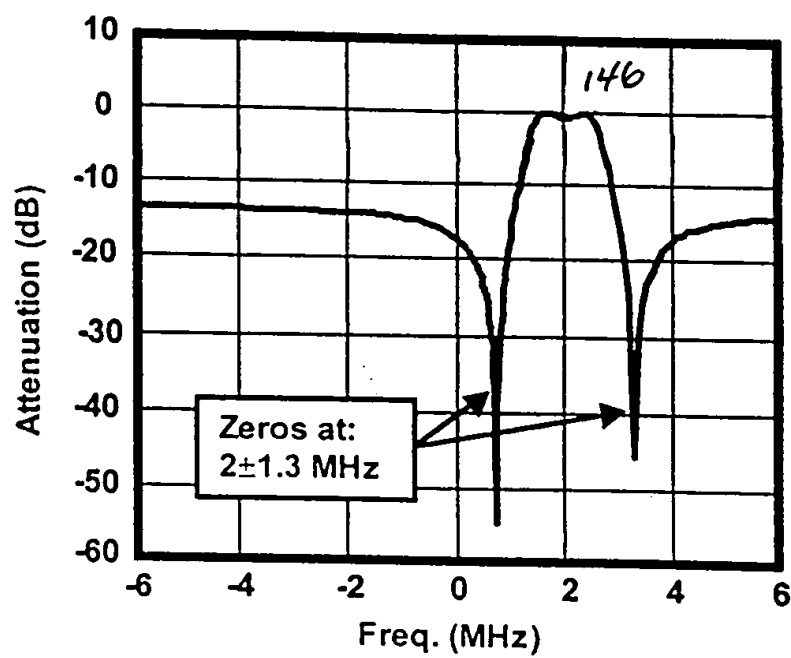


FIG. 11

Diagram of a 4-bit parallel adder using four 1-bit full adders. The inputs are  $C_u/12$ ,  $C_u/12$ ,  $C_u/14$ ,  $C_u/18$ , and  $C_u/16$ . The outputs are 148, 150  $S_1$ , 152  $S_2$ , 154  $S_3$ , and 156  $S_4$ .

FIG. 12(b)

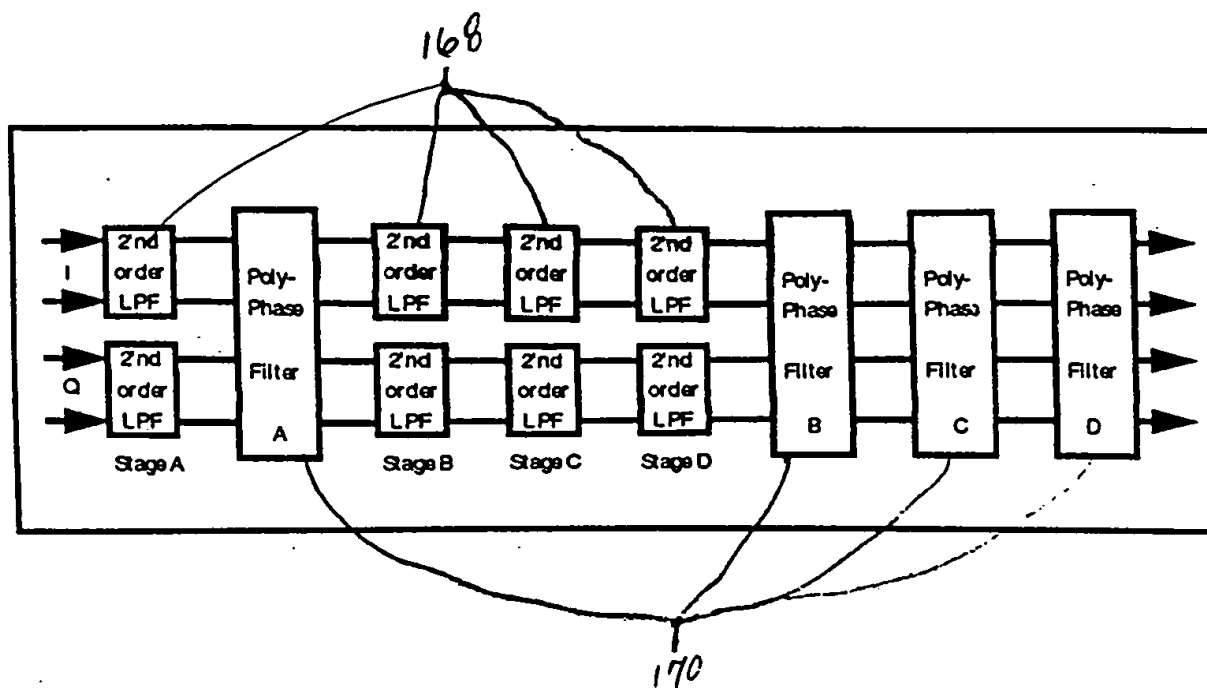
[illegible]

FIG. 13

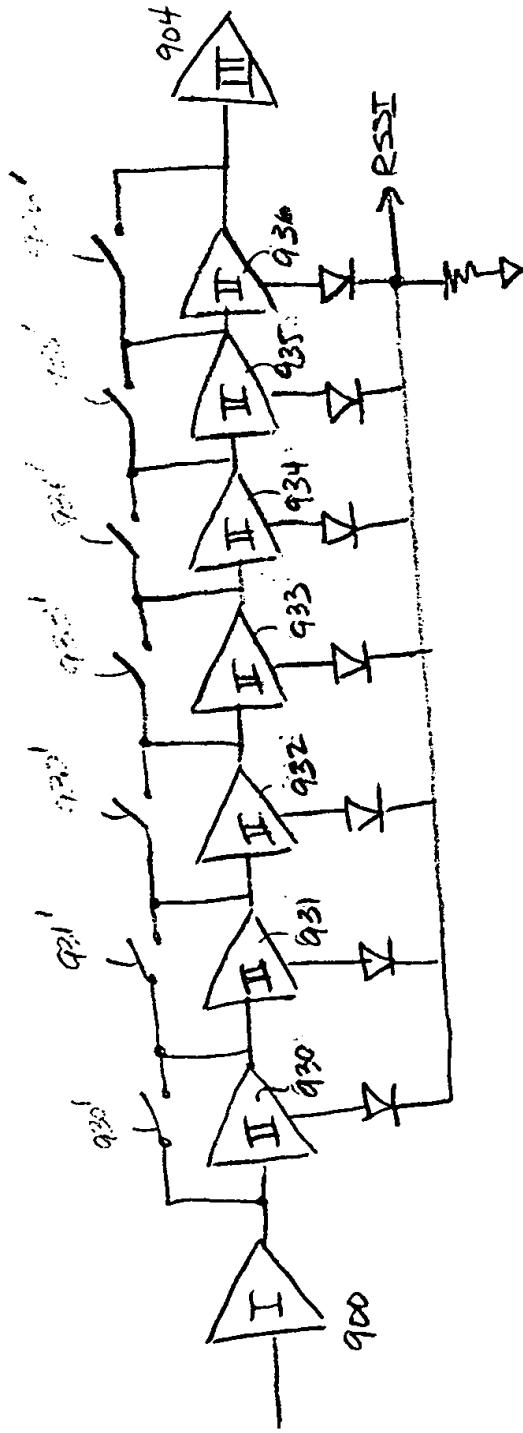


FIG. 14

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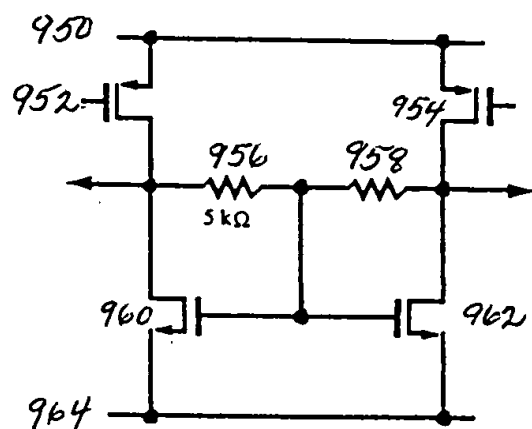


FIG. 15

FIG. 16(a)



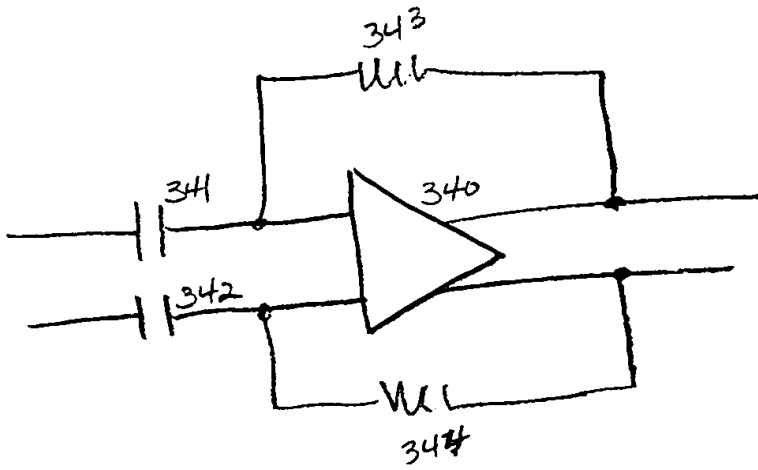


FIGURE 22

09634552-000800

FIG. 16(b)

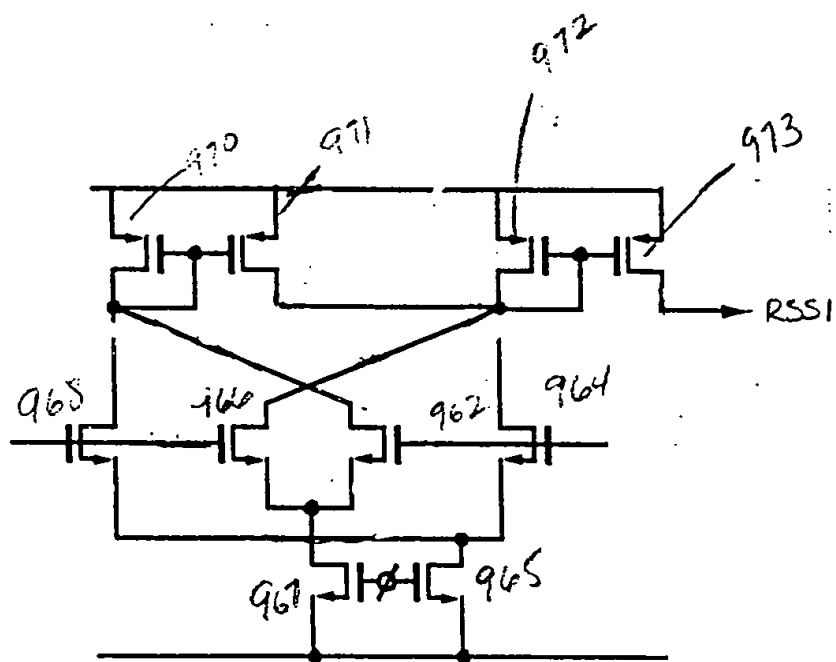


FIG. 17(a)

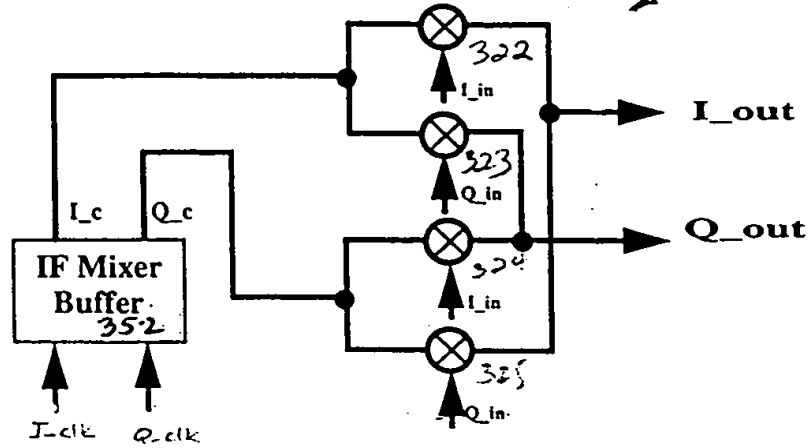


FIG. 17(b)

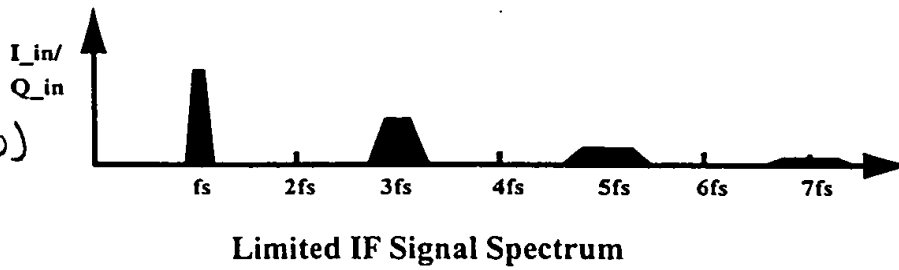


FIG. 17(c)

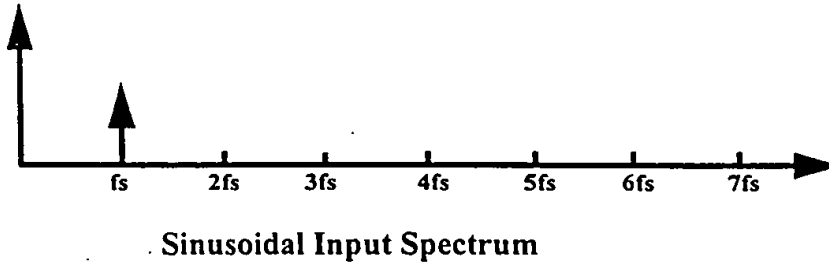


FIG. 17(d)

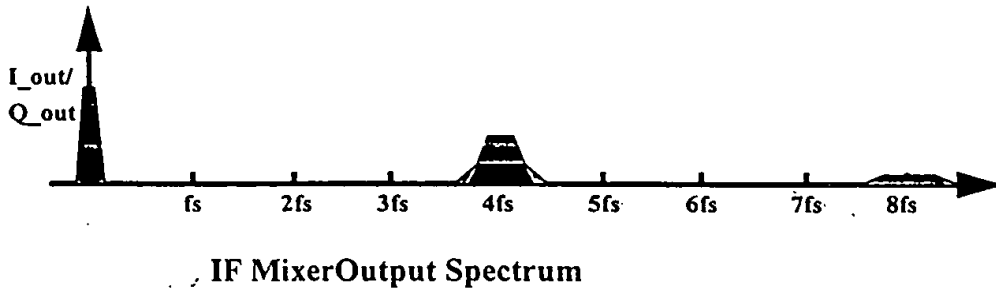


FIG. 18

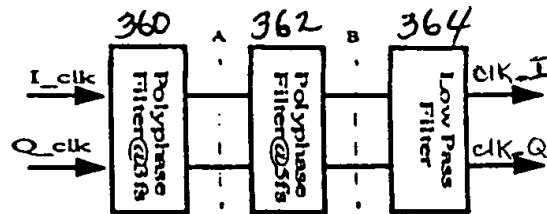


FIG. 19(a)

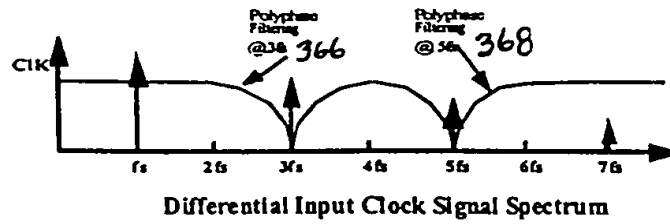


FIG. 19(b)

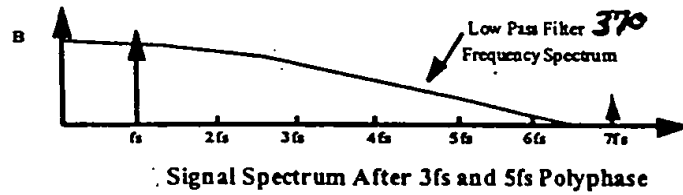
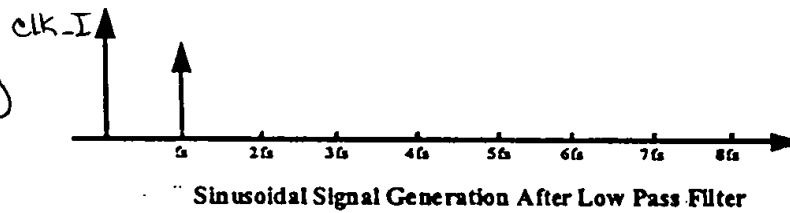
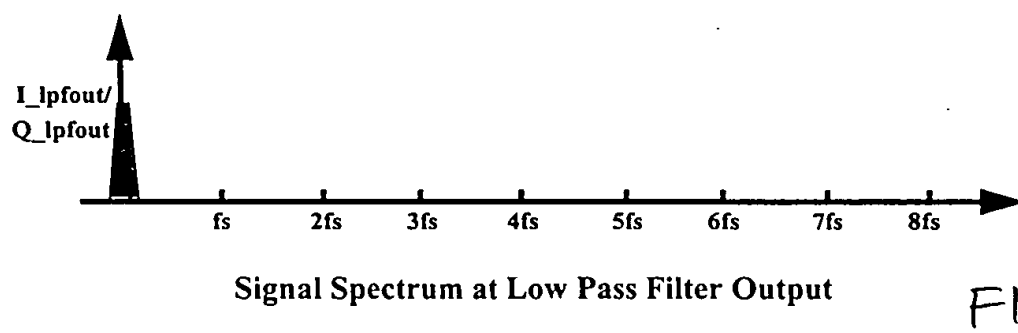
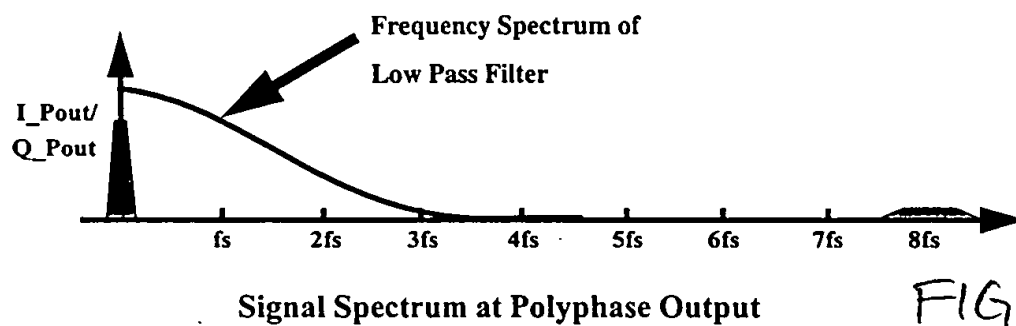
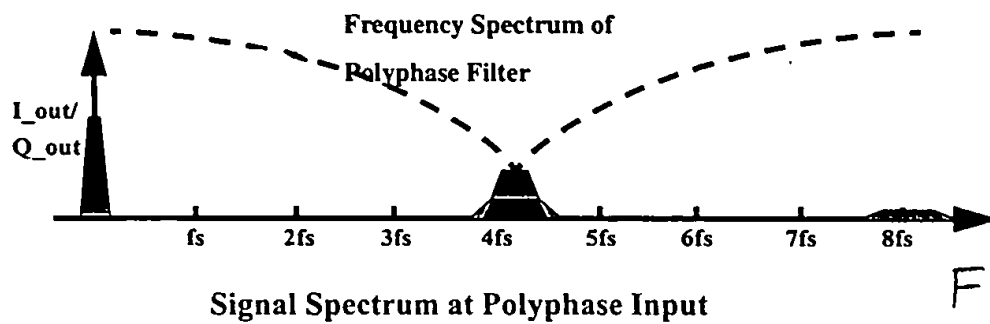


FIG. 19(c)





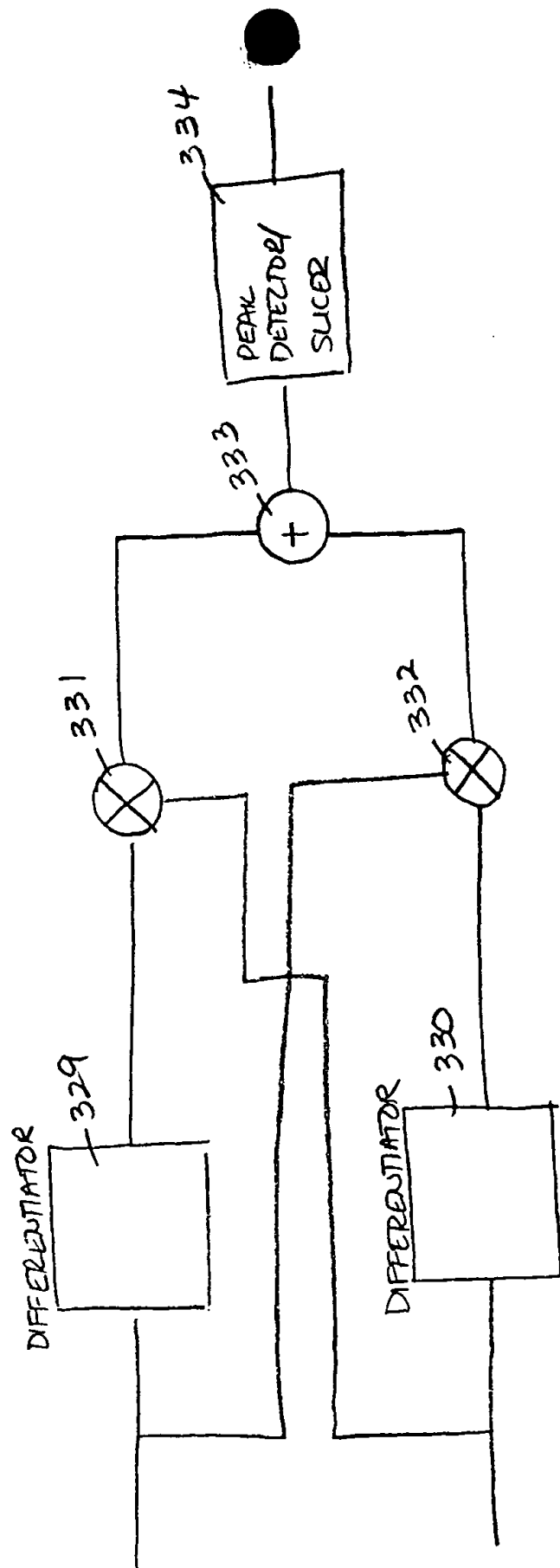


FIG. 21

09634552 020800

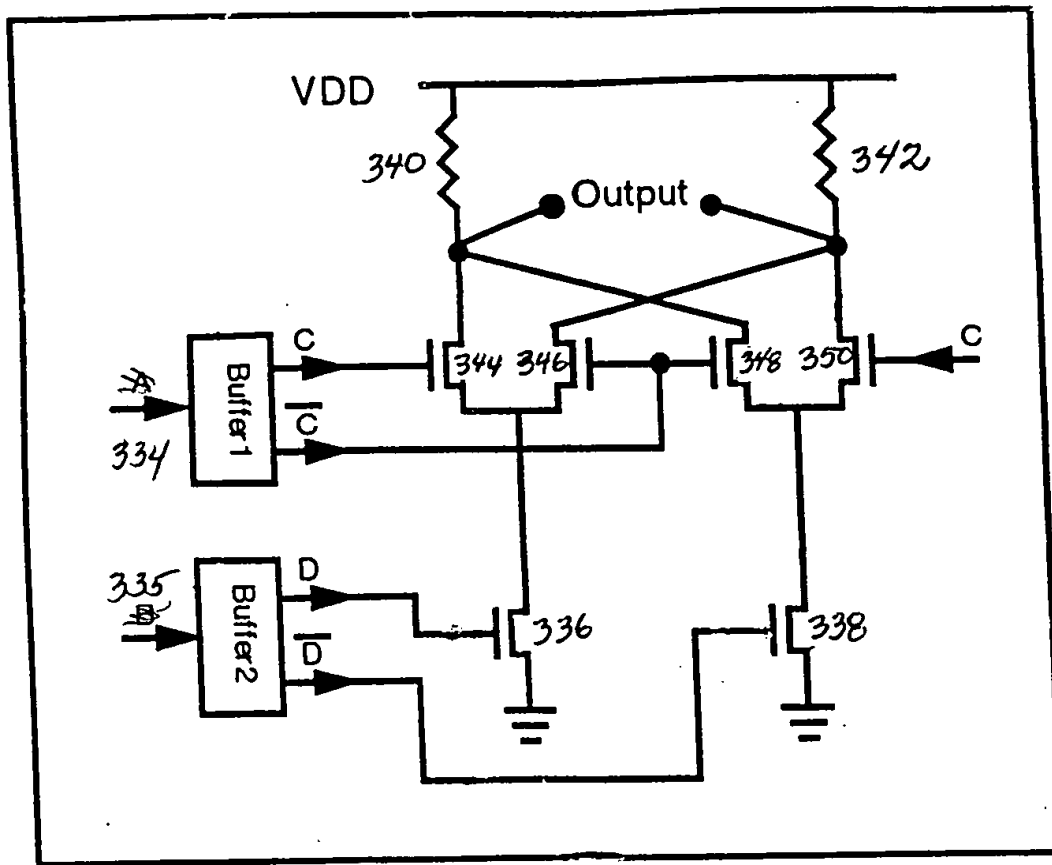


FIG. 23

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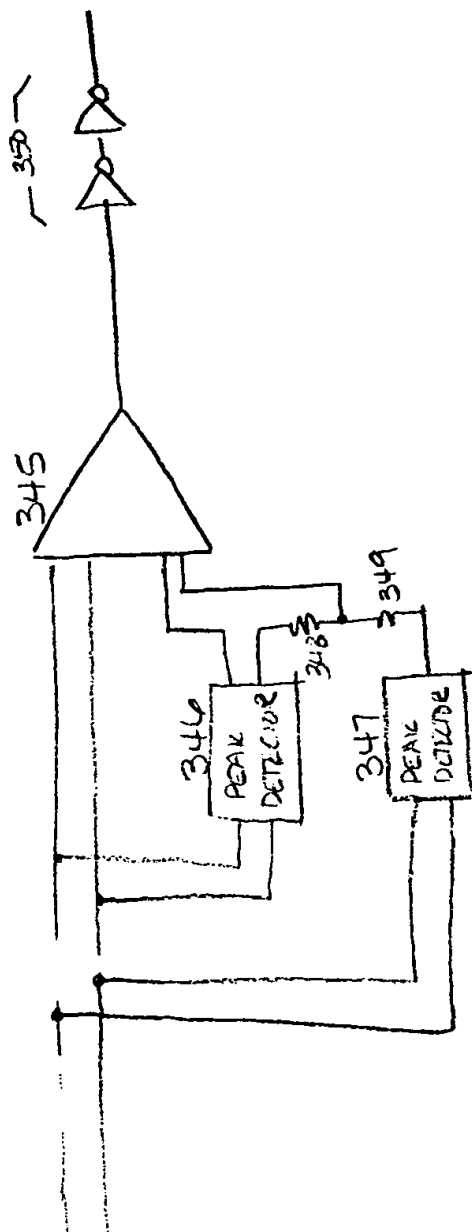


FIGURE 24



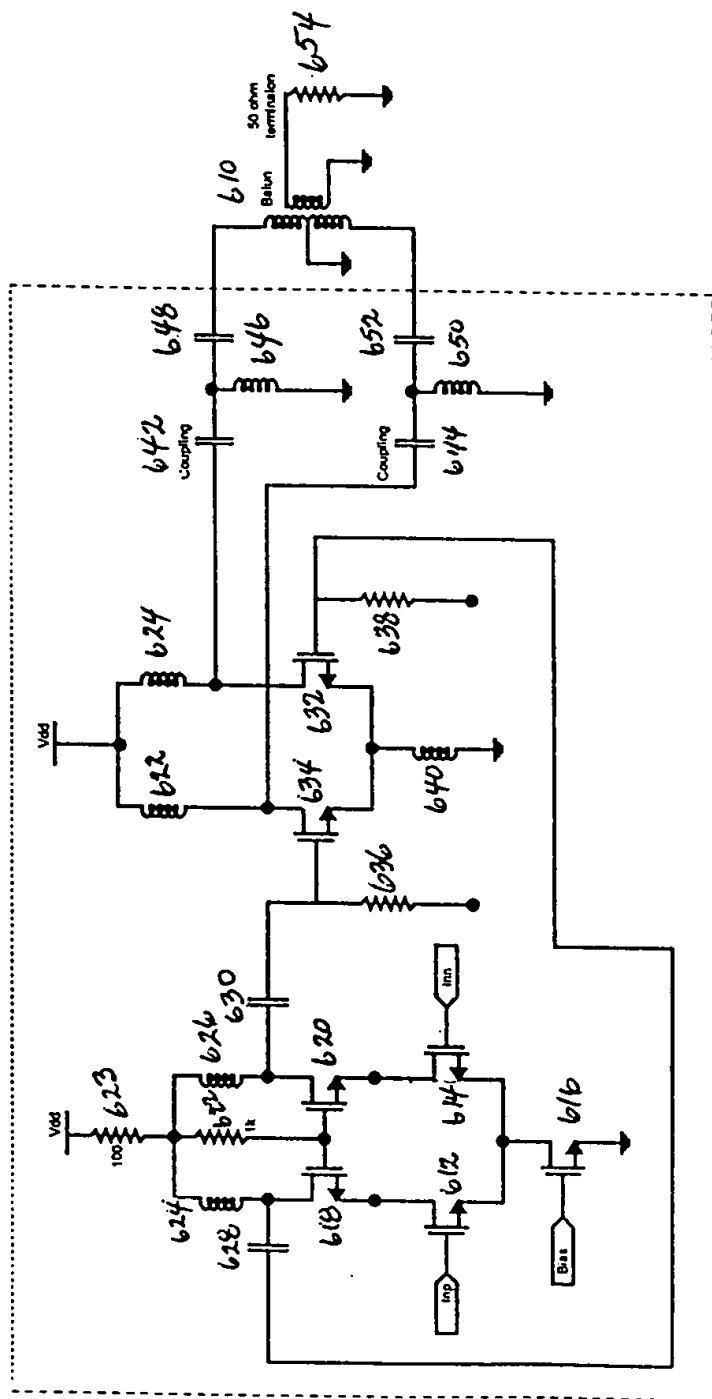


FIG. 25

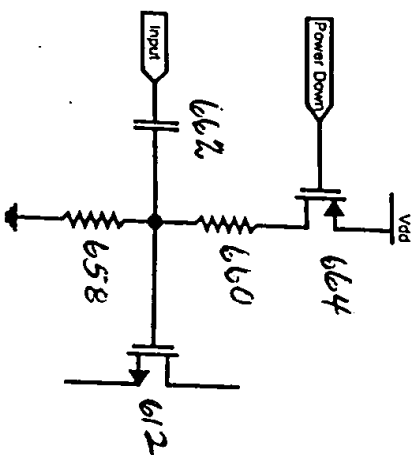


FIG. 26(a)

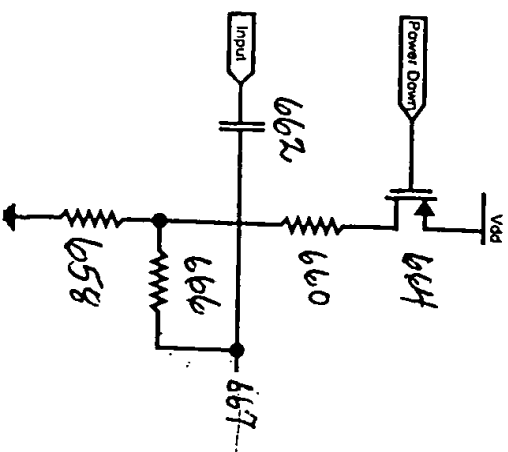


FIG. 26(b)

FIG. 27

**THE UNIVERSITY OF CHICAGO**

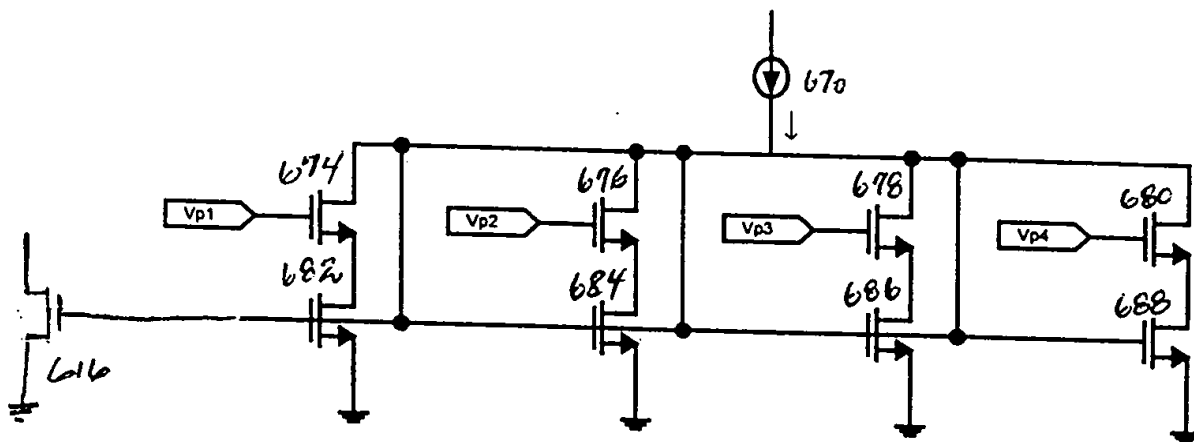


FIG. 28

FIG. 29

000000 " 000000

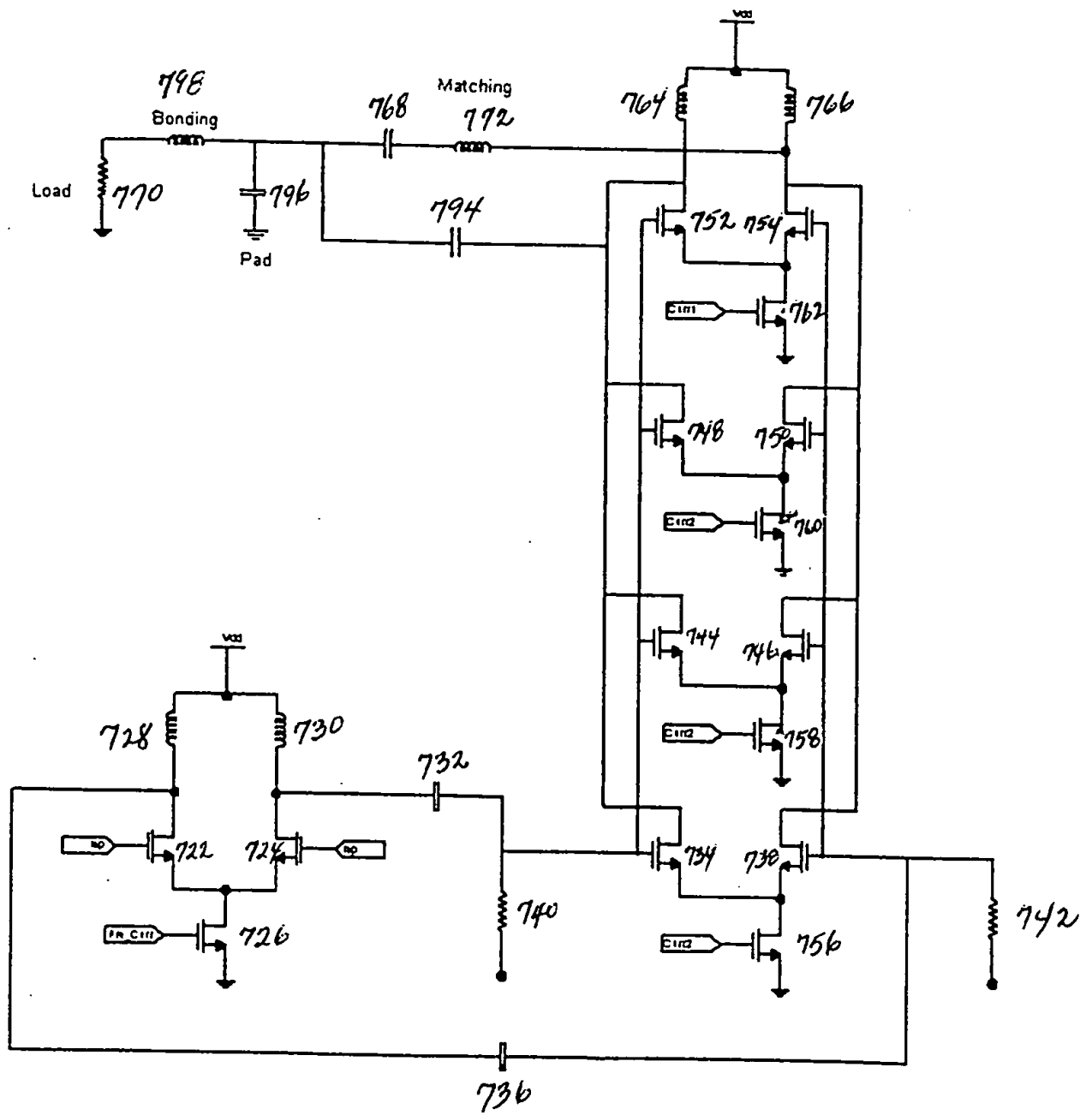


FIG. 30



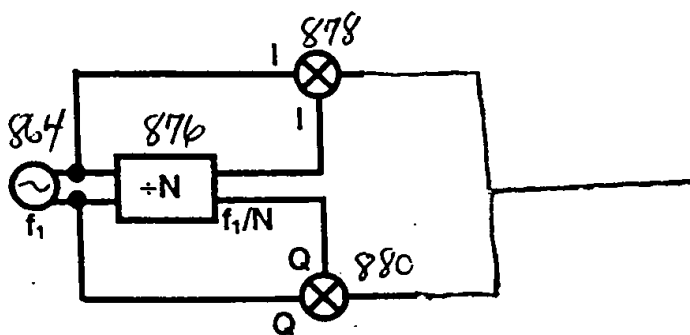


FIG. 32



FIG. 33

# THE UNIVERSITY OF CHICAGO

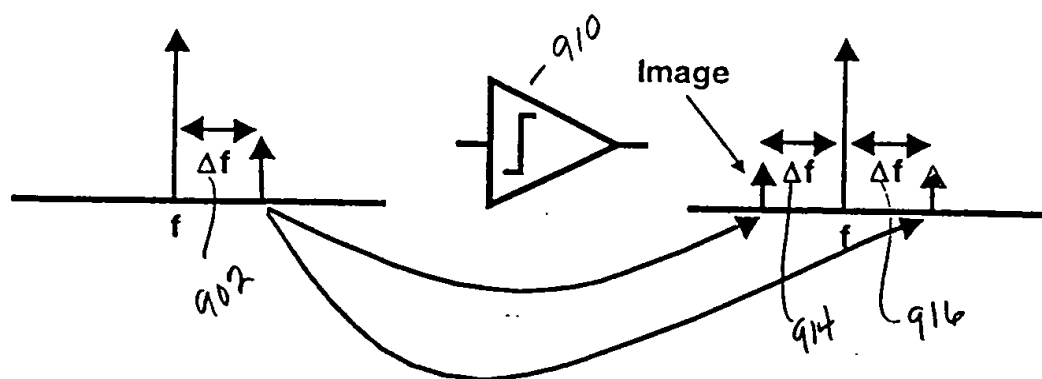


FIG. 33(a)

1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399</
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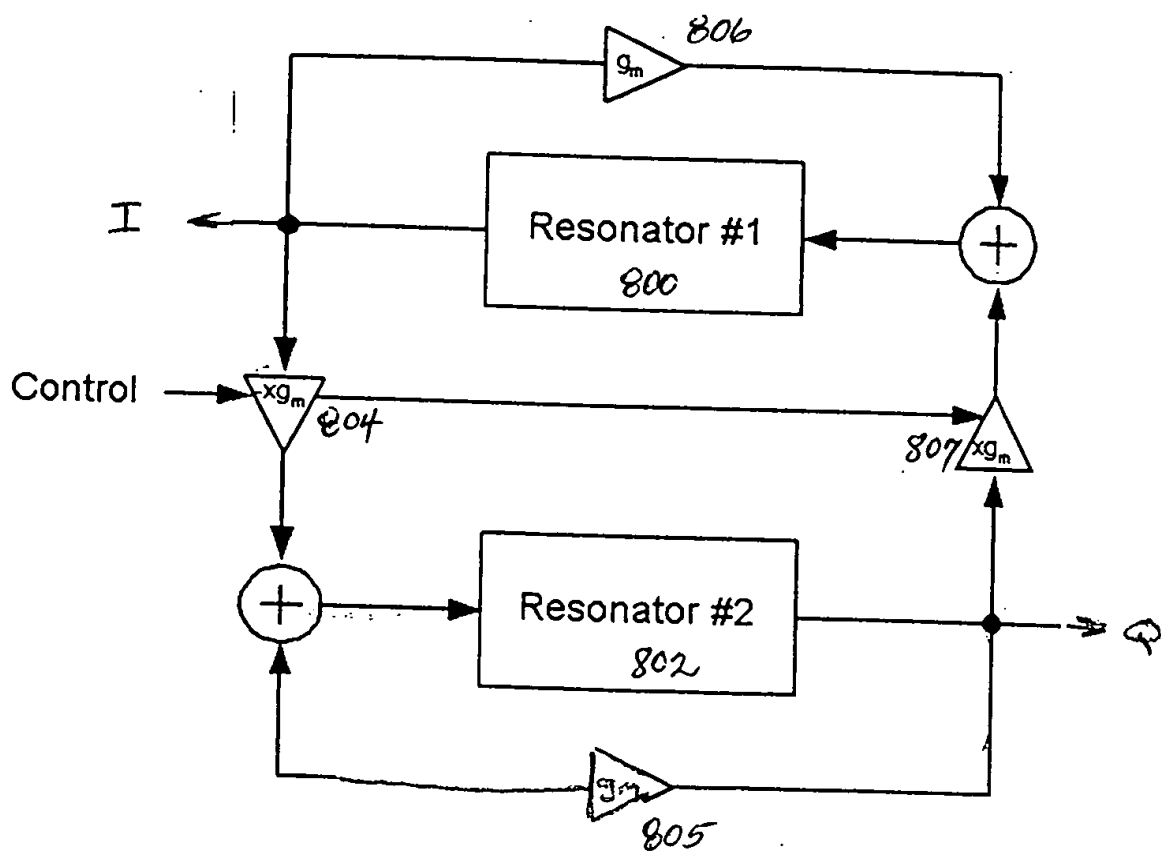


FIG. 34

000000 255452 030000

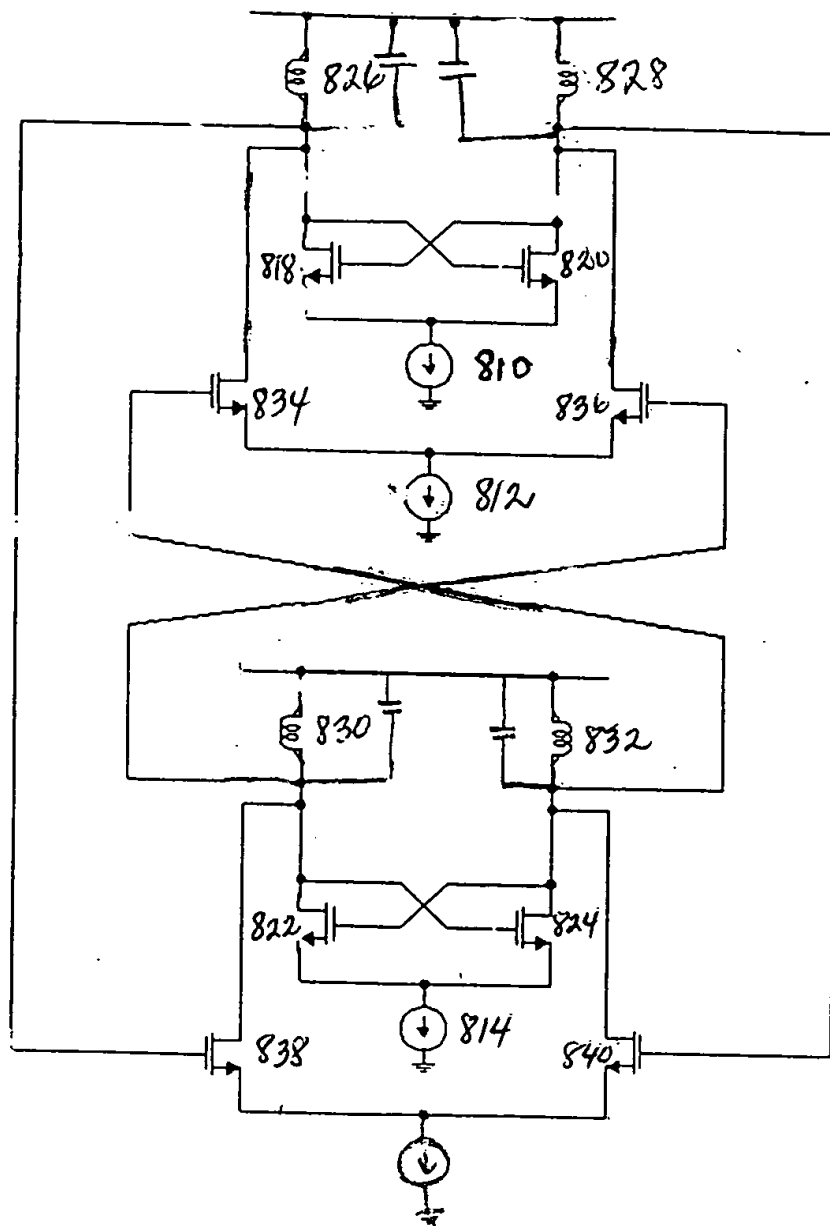


FIG. 35

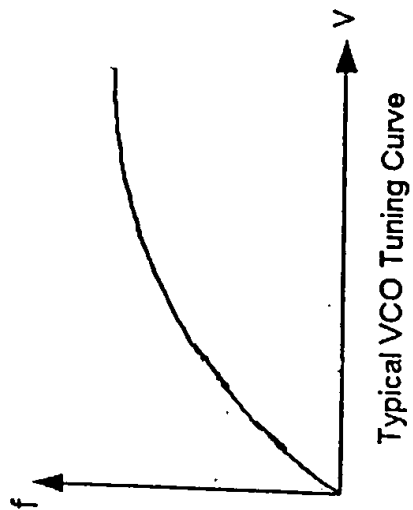


FIG. 36(a)

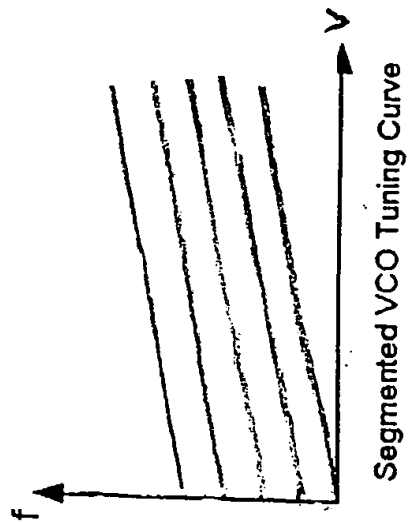


FIG. 36(b)

1. The first part of the paper is devoted to a review of the literature on the topic. It starts with a general introduction to the field of research, followed by a detailed discussion of the various methods and techniques used in the study. The second part of the paper presents the results of the study, which are organized into several sections. Each section discusses a specific aspect of the research, such as the effect of the independent variable on the dependent variable. The third part of the paper is a conclusion, which summarizes the findings of the study and discusses their implications for future research.

FIG. 37(a)

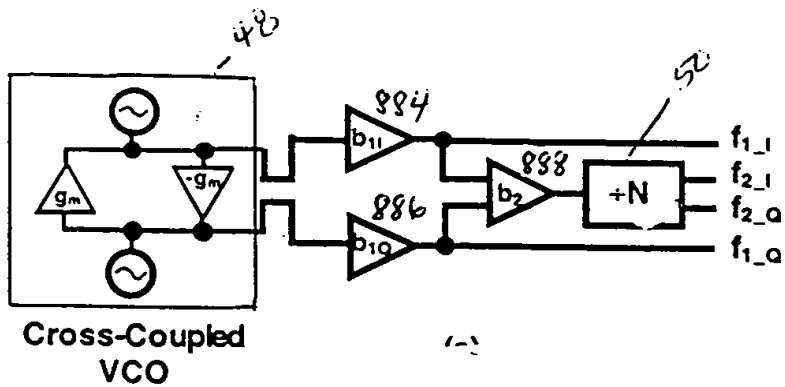
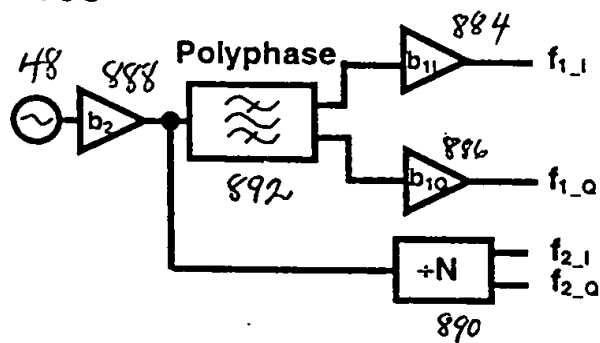


FIG. 37(b)



1. **Содержание**  
 2. **Введение**  
 3. **Глава I. Общие положения**  
 4. **Глава II. Организация и структура**  
 5. **Глава III. Основные задачи и функции**  
 6. **Глава IV. Методы и средства**  
 7. **Глава V. Результаты и выводы**  
 8. **Заключение**  
 9. **Список литературы**  
 10. **Приложения**

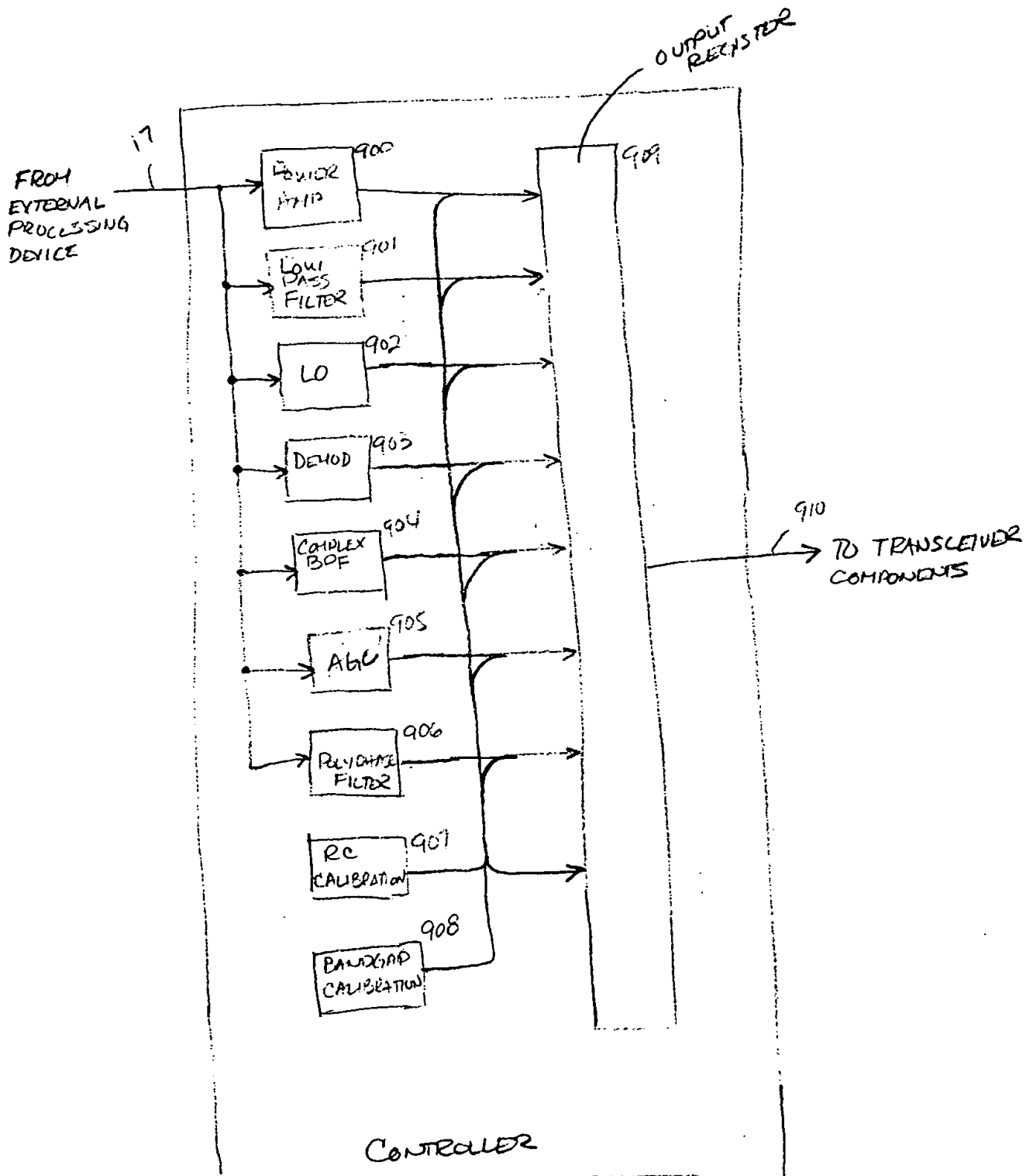


FIGURE 38

**SECRET**

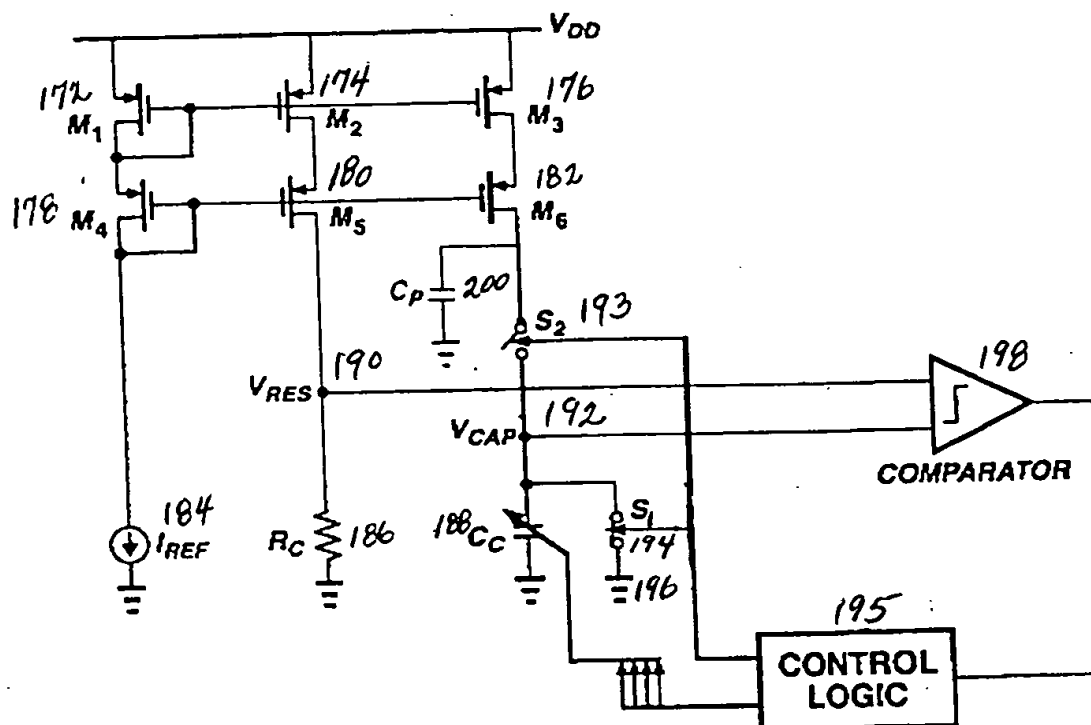


FIG. 39



FIG. 1 is a block diagram of a PLL circuit. The input stage (280) receives an input signal  $X_{IN}$  and a reference signal  $I/Q$ . The input signal  $X_{IN}$  is split into two paths: one through a POLYPHASE A block (282) and another through a POLYPHASE B block (282). The outputs of these blocks are  $X_A$  and  $X_B$ , respectively. These signals are then processed by RSSI (Radio Signal Sensing) blocks (284) and a CONTROL LOGIC block (286). The CONTROL LOGIC block (286) receives a clock signal  $CK$  (250 kHz) and provides feedback signals  $\langle C_A \rangle$  and  $\langle C_B \rangle$  to the POLYPHASE A and POLYPHASE B blocks. The RSSI blocks (284) also provide feedback signals to the CONTROL LOGIC block (286). The output of the CONTROL LOGIC block (286) is fed back to the input stage (280) through a summing junction (288).

FIG. 40

09034592 080800

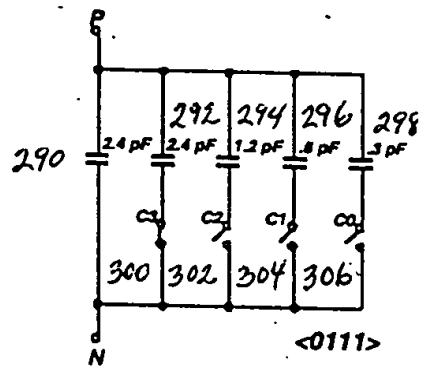


FIG. 41

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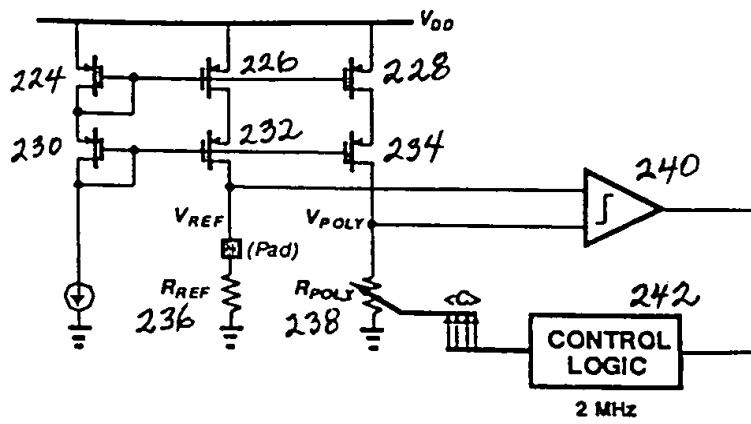


FIG. 42

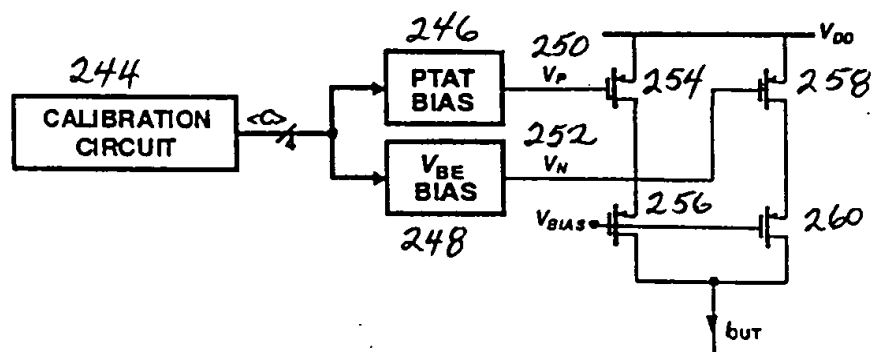


FIG. 43

FIG. 44

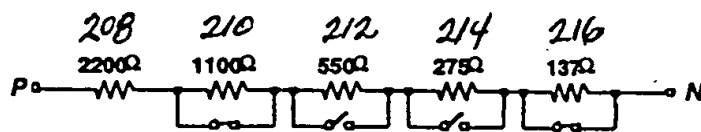


FIG. 45



FIG. 47

